# Receiver with Advanced BITE and Programmable STC for RAWL 02 MK IIA

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***Abstract:***

***Indigenously developed MMIC based double super heterodyne Receiver of RAWL 02 MK IIA is configured to meet Radar requirements of low noise figure, high dynamic range, low phase noise and better sensitivity. Receiver is enabled with advanced BITE facilities which support system calibration. The LNA at the front end of the Receiver has a built-in programmable Sensitivity Time Control to avoid Receiver saturation.***

***Keywords:-Built In Test Equipment, Sensitivity Time Control, Dual channel receiver, low noise figure, high sensitivity, spurious free dynamic range***

## I INTRODUCTION

Receiver of RAWL 02MK IIA is a state-of the art super heterodyne system designed for medium range L Band 2D air surveillance pulse compression Radar for ship borne or onshore applications. Ultra low phase noise Receiver frontend is provided with Sensitivity Time Control (STC) at Low Noise Amplifier (LNA) and TR Limiter to keep the Receiver saturation under control, thus enabling the Radar to meet in excess the target detection range specification. High harmonics/spurious rejection (better than 70dBc), superior Minimum Detectable Signal (MDS) performance upto -110dBm (1.000e-008 µW), low Noise Figure of 3dB has provided an upper hand to the Radar performance. Receiver is enabled with online health monitoring facilities, agility modes of operation and system offline calibration options at the Radar Controller. This technologically superior Receiver has a wide input dynamic range and ensures better sensitivity.

## II RECEIVER REALIZATION

The Receiver of RAWL 02 MK IIA is designed to meet the Radar requirements of low noise figure, high dynamic range, ultra low phase noise, better spurious/harmonics rejection and better sensitivity. Receiver scheme comprises of main sub modules like Low Noise Amplifier, low phase noise Synthesizer, Downconverter (30MHz) and L-band Upconverter. ***Phase coherency*** for the system is achieved by using reference source for the system as a low phase noise, highly stable OCXO from which the system clocks and local oscillator frequencies are derived. High power amplifier of the transmitter is thus driven by a highly stable RF source. This ***'Dual channel Receiver'*** is configured for Main and SLB channels. Functional block diagram of the Receiver Unit is shown in Figure 1.

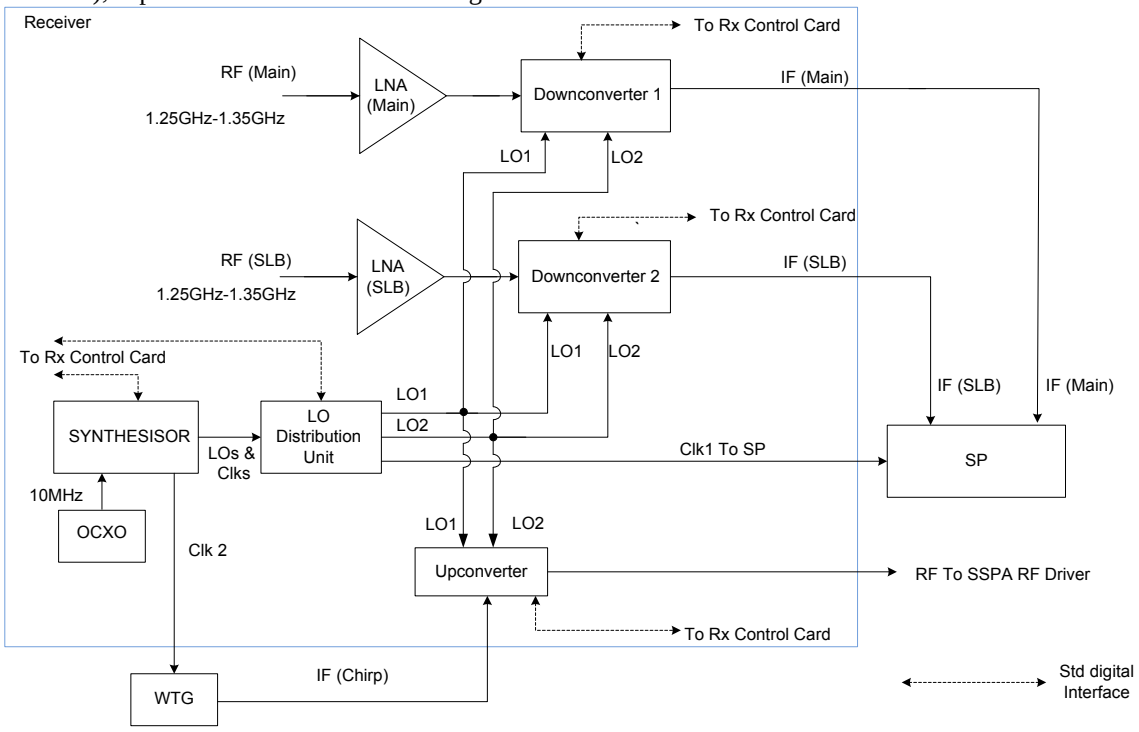


Figure 1: Functional Block Diagram

### *1 Functional Description*

LNA (Figure 2 and Figure 3) which comprises the front end of the double conversion Receiver has a built-in STC adjustment. This will prevent Receiver from going to saturation during high power reflections from clutter and nearby targets thus improving the overall Spurious Free Dynamic Range (SFDR) of the Receiver. A low noise LNA has been used to ensure an overall Receiver chain noise figure less than 3dB. Measured LNA performance is shown in Figure 4 and Figure 5. As a result the system has a better minimum detectable signal and has a good sensitivity.

The received signal from antenna is down converted to 30MHz IF signal and provided to Signal processor for further processing. The down converter modules (Figure 6) have better image rejection and harmonics/spurious levels by virtue of the configuration and band pass filters selected.

High speed switching (settling time less than 0.4µs) Synthesiser Unit (Figure 7) with OCXO as the reference input generates variable L band LO, UHF LO and clock signals for Signal processor and Waveform Generator. Combined PLL and DDS synthesisers and transistor multiplication methods are used for transmitter.

Figure 2: LNA (Module)

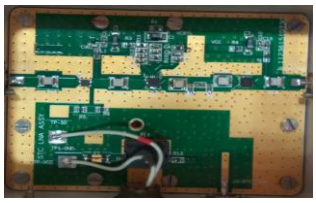

Figure 3: LNA (PCB)


Figure 4: Measured S parameter results of LNA

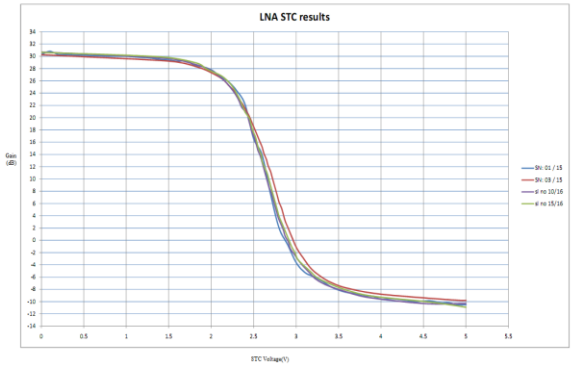


Figure 5: Measured STC performance of LNA

Local oscillator and Receiver clock signals generation respectively. This fast settling ultra low phase noise synthesiser has settling time less than 0.4µs (Figure 8). According to the spot transmission frequency channel selected, Radar Controller provides the control signal to the Synthesiser Unit to generate the corresponding Local Oscillator frequency to both Upconverter and Downconverter Units. Two agility modes of operation (Pseudo Random and Burst to Burst) can also be selected from Radar Controller.

LO distribution unit (Figure 8) distributes Local Oscillator frequencies with appropriate isolation and ensures required drive levels for mixers in the Upconverter and Downconverter units. The unit uses isolators and band pass filters to avoid coupling and interferences. Variable LO signal is generated as per the selection of transmission frequency in the Radar Controller. The same LO signals are used for up conversion and down conversion, thus the system is phase coherent.

The Upconverter unit (Figure 9) has a wide bandwidth of 100MHz and operates on any selected spot frequency. Better image rejection is achieved by using a double super heterodyne conversion scheme in the Upconverter to generate L band signal for transmission using the Linear Frequency Modulation (LFM) signal received from waveform generator. By using mixers with adequate LO rejection and use of necessary band pass/ low pass filters, a low level of spurious is obtained in the L band input provided for transmission.

Figure 6: Downconverter Unit

Figure 7: Synthesiser unit

Figure 8: Top side (left) and rear side (right) of LO Distribution Unit

Figure 9: Upconverter unit

### *2 Realization of RF modules*

The realization of the functional RF modules is done using MMIC devices mounted on **multilayer RF PCBs**. The PCBs have gold plating and are realized on Teflon substrate. Edge plating is provided to ensure seamless grounding of the PCB. The PCBs are impedance matched to operate at high frequency. State-of the art surface mount devices viz amplifiers, mixers, filters etc have been chosen which ensures the module performances. Board mount connectors have been provided enabling the verification of signals at PCB level. Flexible RF cables are used to connect the signals to the box mount connectors.

Each module has an RF PCB and a digital PCB mounted in ***milled Aluminum enclosures*** and are isolated using separation wall. Isolation between different signal chains in the RF PCB is achieved by partitions built into the housing. Grooves are provisioned in the box base to isolate the signal tracks on rear side of the PCB from ground plane.

A generic ***microcontroller based digital PCB*** ported with specific software is designed for each module to exchange controls and status with the Radar Controller. The status of important parameters are monitored and displayed in Radar controller GUI. Digital PCB has got a voltage regulator which supplies ***regulated and EMI filtered power supply*** to the RF devices thus shielding from any minor voltage fluctuations in the system. Standard serial interface has been realized enabling the standalone verification of the communication to Radar Controller using simulators.

## III BITE IMPLEMENTATION

Receiver communication with Radar Controller is through LAN interface. Online health status monitoring (Figure 10) of the unit is made possible by capturing and monitoring the important status parameters of various Receiver modules. Thus by monitoring crucial parameters like LO Distribution Unit output power levels and Synthesiser locking to reference OCXO, which are crucial for driving the mixers of Upconverter and Downconverter modules and maintaining coherency of the system respectively, stable and accurate Radar performance is ensured.

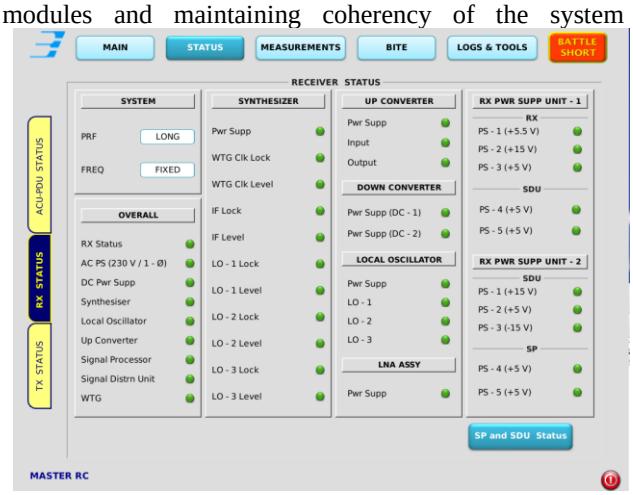


Figure 10: Receiver status page of Radar Controller

### *3 Receiver Calibration*

Receiver is designed with in-built dynamic range plotting option which is controlled from Radar Controller. The instructions from the Radar Controller are given through LAN connectivity to the external signal generator connected to the LNA input. Frequency and power level selections are available in Radar Controller. The input power level of signal generator is varied over the dynamic range. Then the detected analog output power values are plotted in Radar Controller showing dynamic range of the Receiver (Figure 11). Facility to zoom in the plot is also available.

### *4 Noise Figure Measurement*

A facility is available for measuring Noise Figure of the Receiver in offline mode. A wideband noise signal is injected through a directional coupler before the LNA. The noise figure is measured using 'Y Factor' method and displayed in the Radar Controller. The command to start Noise Figure measurement is sent from Radar Controller in offline mode.

## IV RECEIVER"SENSITIVITY TIME CONTROL" HARDWARE AND SOFTWARE

Hardware with Xilinx Virtex 5 FX Series FPGA is designed and developed for generation of Programmable waveforms for controlling gain of LNA and TRL modules for STC functionality. Real time soft control adjustment of gain of the LNA is available for both Short and Long pulses. Software takes care of auto-adjustment depending on RPM and modes of Radar. User friendly GUI control available in the Radar Controller enables the user to adjust the STC amplitude, pulse duration and slope type according to the current target scenario.

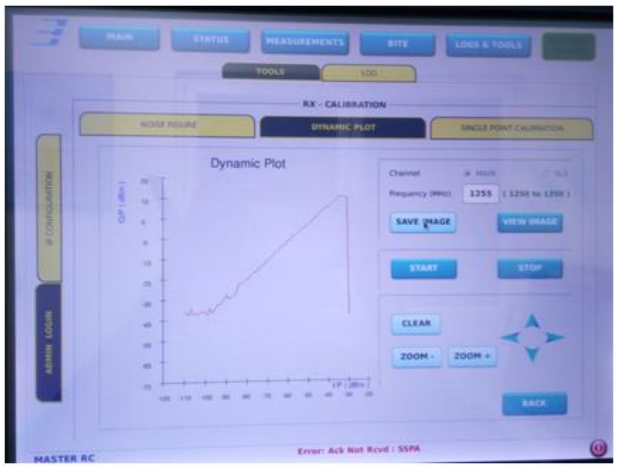


Figure 11: Dynamic Plot

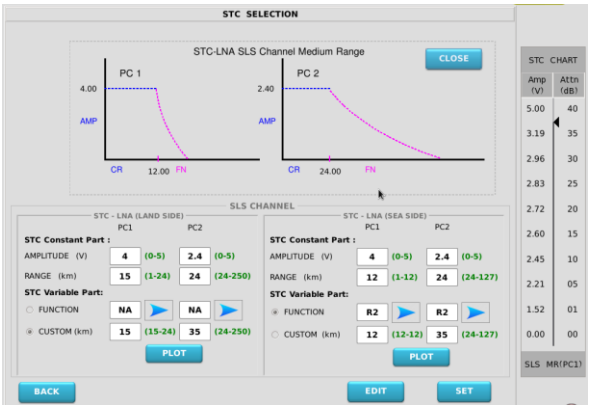


Figure 12: STC Page of Radar Controller

Figure 13: STC Hardware (Xilinx Virtex 5)

STC signals with programmable amplitude (0 to 5V), constant range width and variable range falling edge width (0 to 300 us) of slant type or curve type of $R^2$, $R^3$, $R^4$ can be generated. Radar controller has a configuration page (Figure 12) for setting above parameters for all three channels. The firmware forms the bridge between Radar controller and STC hardware for communicating various waveforms and triggers parameters for staggered and non-staggered Radar operation modes.

### *5 Hardware Implementation*

STC PCB is a 12 layer board (Figure 13) which generates sensitivity time control signals, for controlling the gain of LNA (Main and SLB channel) and TRL. For generating STC pulses required for gain control of Receiver LNA, the PCB uses 40 Msps DAC. FPGA generates the clock, data input and control signals required for 40 Msps DAC. Four such DACs are interfaced. BRAM elements which are available in FPGA are used for storing co-efficients. Parallel IOs are used for exchange of data from firmware to hardware logic.

### *6 Software Implementation*

Firmware is developed in VHDL and embedded C in Linux environment. The co-efficient required for generating the pulse is calculated at firmware level and is filled to BRAM via parallel IOs. Two BRAMs are used for storing co-efficients of short pulse and long pulse. If any change of pulse characteristics then co-efficients are recalculated and stored to BRAM. The transmitted sync triggers for short and long pulse are used as reference by VHDL logic for reading the co-efficients from BRAM and feeding those into 16 bit DAC input. Analog output of DAC is fed to op-amp for I to V conversion and final output is available in 50 ohm SMA connector. STC pulses are synchronized with the radar triggers. Ethernet interface is available for online change of pulse profiles via Radar controller.

## CONCLUSION

Receiver of RAWL-02 Mk IIA Radar is indigenously designed, developed and tested inhouse.

- Indigenous development of Dual channel receiver
- Coherent system with high dynamic range and better sensitivity
- User friendly online STC adjustment
- Advanced BITE facility for system calibration and online status monitoring

## ACKNOWLEDGMENT

The author would like to specially thank Smt Kalyani Murthy, AGM, RFC/C-D&E, Bharat Electronics Limited, Shri M Ramesh, Senior Research Staff, Central Research Laboratory, Bharat Electronics Limited and Shri Chandrasekaran K, Senior DGM, Naval Systems 2, Bharat Electronics Limited, for their valuable suggestions and extensive support throughout the design and the implementation.

## REFERENCES

[1] Merrill S Skolnik "*An introduction to RADAR","RADAR Handbook", McGrew Hill, Third edition, 2001.*

[2] Bassem R. Mahafza "*Radar Systems Analysisand Design using Matlab", Chapman & Hall/CRC, 2000.*

[3] Hsu-Feng Chou, A. Ramaswamy, D. Zibar, L.A. Johansson, J.E. Bowers, M. Rodwell, and L.A. Coldren, *"SFDR Improvement of a Coherent Receiver Using Feedback,"* OSA topical meeting of Coherent Optical Techniques and Applications (COTA), Whistler, BC, 2006. CFA3.

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